

TSMC's Open Innovation Platform Theatre, **Booth #294**

	Monday	Tuesday	Wednesday	
Morning	09:15 – 09:30	Arteris Improving SoC Success through Arteris NoC Interconnect in TSMC Release 11 Flow	Cosmic Circuits Analog with Certainty	ARM ARM & TSMC Working Together to Accelerate the Future
	09:30 – 09:45	Synopsys DesignWare IP supporting Advanced TSMC Process Technologies	Analog Bits Your Trusted Partner for Differentiation. The Analog Bits of TSMC's Digital Chips	Integrand RF Modeling and Characterization at TSMC using Integrand's EMX
	10:00 – 10:15	Magma Magma – Accelerating Mixed Signal SoC Design	Virage Logic Integration and Verification of Third Party IP	eSilicon Optimizing ROI for Electronics Companies
	10:30 – 10:45	Mentor Mentor Open Innovation Platform Efforts	eSilicon Optimizing ROI for Electronics Companies	Lorentz Peakview: Addressing EM Design and Verification challenges with TSMC
	11:00 – 11:15	Cadence Leading edge Silicon Realization solutions for advanced node mixed-signal designs	MoSys MoSys and TSMC Collaborating for Innovation	Cadence TLM Design & Verification – Moving the golden source from RTL to TLM
	11:30 – 11:45	TSMC Open Innovation Platform Phase 2	TSMC Open Innovation Platform Phase 2	TSMC Open Innovation Platform Phase 2
Lunch	12:00 – 12:15	Apache Power Integrity and Reliability Signoff using Apache's Tools	Tela Innovation Reducing Power and Area with PowerTrim and AreaTrim	Helic A full featured EM aware high speed/RF IC design methodology – Reduce die area, design time & risk.
	12:30 – 12:45	Helic A full featured EM aware high speed/RF IC design methodology – Reduce die area, design time & risk.	Solido Variation-Aware Custom IC Design with Solido Variation Designer	MoSys MoSys and TSMC Collaborating for Innovation
Afternoon	01:00 – 01:15	eSilicon Optimizing ROI for Electronics Companies	Cadence Delivering Silicon Realization productivity for Giga-Gate, Giga-Hertz Designs	Synopsys Interoperable PDKs enable Advanced Analog Design Automation
	01:30 – 01:45	Solido Variation-Aware Custom IC Design with Solido Variation Designer	Lorentz Peakview: Addressing EM Design and Verification challenges with TSMC	Magma Magma – Accelerating Mixed Signal SoC Design
	02:00 – 02:15	Silicon Frontline 3D Extraction and Analysis for Advanced Process Technology	Helic A full featured EM aware high speed/RF IC design methodology – Reduce die area, design time & risk.	Mentor Mentor OIP Efforts
	02:30 – 02:45	Springsoft Custom IC flow with layout dependent effect (LDE) constraints and checking at 28nm	Integrand RF Modeling and Characterization at TSMC using Integrand's EMX	Apache Power Integrity and Reliability Signoff using Apache's Tools
	03:00 – 03:15	Analog Bits Your Trusted Partner for Differentiation. The Analog Bits of TSMC's Digital Chips.	Synopsys In-Design Physical Verification for Faster Time to Tapeout	Tela Innovation Reducing Power and Area with PowerTrim and AreaTrim
	03:30 – 03:45	Virage Logic Virage Logic's Extensive SiWare™ Memory Compiler Portfolio	Magma Magma – Accelerating Mixed Signal SoC Design	Solido Variation-Aware Custom IC Design with Solido Variation Designer
	04:00 – 04:15	Tela Innovation Reducing Power and Area with PowerTrim and AreaTrim	Mentor Shorten your Schematic/Layout Loop with IC Station (TSMC Reference Flow 11)	Silicon Frontline 3D Extraction and Analysis for Advanced Process Technology
	04:30 – 04:45	MoSys MoSys and TSMC Collaborating for Innovation	Apache Power Integrity and Reliability Signoff using Apache's Tools	Springsoft Custom IC flow with layout dependent effect (LDE) constraints and checking at 28nm
	05:00 – 05:15	Integrand RF Modeling and Characterization at TSMC using Integrand's EMX	Silicon Frontline 3D Extraction and Analysis for Advanced Process Technology	Analog Bits Your Trusted Partner for Differentiation. The Analog Bits of TSMC's Digital Chips.
05:30 – 05:45	Lorentz Peakview: Addressing EM Design and Verification challenges with TSMC	Springsoft Custom IC flow with layout dependent effect (LDE) constraints and checking at 28nm	Virage Logic Power Optimization with Virage Logic Standard Cell Logic Blocks	



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